REMARKS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-6 and 14 are presently active in this case. The present Amendment amends Claim 1 without introducing any new matter; and cancels Claims 7-13 without prejudice or disclaimer.

In the outstanding Office Action, Claims 1-3 and 14 were rejected under 35 U.S.C. §§102(a) or 102(e) as anticipated by Asao et al (U.S. Patent No. 6,590,244, herein "Asao"). Claims 4-5 were rejected under 35 U.S.C. §103(a) as unpatentable over Asao in view of Pan et al. (U.S. Patent 6,548,849, herein "Pan"). Claim 6 was rejected under 35 U.S.C. §103(a) as unpatentable over Asao in view of Scheuerlein et al. (IEEE Publication, February 2000, International Solid State Circuits Conference, herein "Scheuerlein").

In response to the Restriction Requirement being made final in the August 8, 2005 Office Action, Claims 7-13, directed to non-elected inventions, are canceled. Applicant reserves the right to present claims directed to the non-elected inventions in a divisional application, which shall be subject to the third sentence of 35 U.S.C. §121.[1]

To clarify Applicant's invention, Claim 1 is amended to recite "the magnetic layer insulated from either the third wiring line or the fourth wiring line by an insulator film, wherein the insulator film is an interlayer insulator film." This feature finds non-limiting support in Applicant's disclosure, for example from page 31, line 11, to page 32, line 19, and in corresponding Figure 24, reference numerals 27b and 116_{-1}.

[1] "A patent issuing on an application with respect to which a requirement for restriction under this section has been made ... shall not be used as a reference ... against a divisional application." See also MPEP 804.01.

In light of the amendments to independent Claim 1, Applicant respectfully request reconsideration of the rejection of Claims 1-3 and 14 under 35 U.S.C §§102(a) and 102(e), and traverses the rejection, as next discussed.

Briefly summarizing, Applicant's Claim 1, relates to an MRAM (Magnetic Random Access Memory) using an MTJ (Magnetic Tunnel Junction) structure as storage elements. As a non-limiting application example of Applicant's invention as specified in Claim 1, a magnetic layer (magnetic material) is used to form a TMR (Tunneling Magneto Resistive) element for the purpose of suppressing generation of inductance components due to the proximity of wiring lines in *a peripheral circuit* as a result of the close arrangement of the bit lines and the write word lines. The bit lines and write word lines are usually arranged close to each another so as to allow the use of a smaller write current, to decrease power consumption.

More specifically, Claim 1 provides, *inter alia*, an MTJ film 27b composed of a fixed magnetic layer $116._1$ and an insulator film 16 as an interlayer insulator film on a wiring line 20c in the fourth level of *a core peripheral circuit*, such that the wiring line 20c in the fourth level and a wiring line 21c in the fifth level are ***not electrically connected***, see for example Applicant's Figures 24, 40 and 41.

Claim 1 improves upon background magnetic memory devices, since with the above-described structure, it is possible not only to suppress parasitic inductance in the core peripheral circuit and reliably perform a CMP (Chemical Mechanical Polishing) processing for flattening the insulator film 16, but also it is possible to keep a complete insulation state between the wiring line 20c in the fourth level and the wiring line 21c in the fifth level via the insulator film 16. In a non-limiting example shown in Applicant's Figure 1, the magnetic memory device includes a resistive element 30 composed of a magnetization fixing layer 41, a tunnel junction 42, and a magnetic recording layer 43.

Turning now to the applied references, Asao describes a memory cell section, wherein a second magneto resistive effect element of a peripheral circuit, which is disposed between the fourth and fifth wirings, is also ***connected to*** the fourth and fifth wirings to be used as a resistive element.[2] Asao's peripheral circuit is configured such that upper and lower wiring lines 20b and 19b are connected to each other via resistive element 30 (TMR element 25b). However, Asao fails to teach or suggest that the magnetic layer insulated from either the third wiring line or the fourth wiring line by an insulator film, wherein the insulator film is an interlayer insulator film, as recited in amended, independent Claim 1. Asao clearly shows in Figure 1 the element 30(25b) being electrically connected to the wiring lines 19b ***and*** 20b. The structure of the TMR element 25b is further detailed in Asao's Figures 4a-4a and 5a-5b. Such structure can be seen throughout Asao's Figures and passages in the specification.

Therefore, Asao fails to teach or suggest every feature recited in amended, independent Claim 1, so that Claims 1-3 and 14 are believed to be patentably distinct over Asao. Accordingly, Applicant respectfully traverses, and requests reconsideration of, the rejection based on Asao.[3]

The reference Pan and Scheuerlein, relied upon by the outstanding Office Action as secondary references to form a 35 U.S.C. §103(a) of the dependent claims, does not remedy the deficiencies of Asao, as next discussed.

The reference Pan describes an MRAM device that includes a magnetic tunneling junction MTJ stacks 12, with a pair of magnetic yoke structures, arranged on a word line 20.[4] However, Pan fails to teach or suggest anything on a core peripheral circuit for controlling the memory cell. In Pan's MRAM devices, on top of the MTJ stack, NiFe layers 58, 62 and

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[2] See Asao in the Abstract, lines 10-13.
[3] See MPEP 2131: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," (Citations omitted) (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."
[4] See Pan in the Abstract, and at column 4, lines 43-59, and in Figure 1 and 13.

72 are arranged, forming an *encapsulating structure* 22.[5] Accordingly, Pan fails to teach or suggest the magnetic layer insulated from either the third wiring line or the fourth wiring line by an insulator film, as recited in amended, independent Claim 1.

The reference Scheuerlein describes a magnetic random access memory, and also fails to teach or suggest anything on a core peripheral circuit for controlling the memory cell. Scheuerlein merely discloses a MTJ MRAM device and recites "[t]he lower layers of the MTJ extend to the side and contact the lower wiring layer and the FET. The write word line is below the MTJ to provide a magnetic field for writing."[6] Accordingly, Scheuerlein also fails to teach or suggest the magnetic layer insulated from either the third wiring line or the fourth wiring line by an insulator film, as recited in amended, independent Claim 1.

Therefore, even if the combination of Asao, Pan and/or Scheuerlein is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach the claimed elements of the peripheral circuit including a magnetic layer. Accordingly, Applicant respectfully traverses, and requests reconsideration of, this rejection based on these patents.[7]

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-6 and 14 is earnestly solicited.

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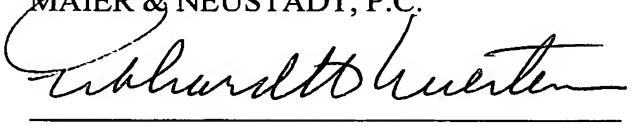
[5] See Pan at column 4, lines 11-28, and in Figures 1, 12 and 13.
[6] See Scheuerlein at page 128, column 1, lines 27-30, and in Figure 7.2.1a.
[7] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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